

In the Specification

Please amend paragraph 0023 as follows:

In a state that the second via hole 107 has been formed, as shown in Figure 5D, a metal layer, i.e., a first metal layer for forming an anti-fuse is formed in a certain thickness on the semiconductor substrate including in the second via hole 107. Then, a conductive metal layer, i.e., a second metal layer is formed on the semiconductor substrate including the first metal layer to sufficiently fill the second via hole. Then, the first metal layer and second metal layer are planarized with the second insulating layer 106. Thus, the anti-fuse 108c is formed in the second via hole 107 and a third contact plug 108b, which is narrower in width than the second contact plug 108a, is formed inside the anti-fuse.

Please replace Figures 4 and 5D with the corrected drawings sheets attached hereto.